REMARKS/ARGUMENTS

Claims 10 through 16 and 22 through 32 remain in the application. Claims 10 through 13, 16 and claims 22 through 32 have been amended. The Applicant would like to thank the Examiner for his diligent examination.

The Abstract has been amended to incorporate the suggested amendment as outlined in the Detailed Final Action.

Referring to paragraph [0062], the Applicant has amended a portion of this paragraph to recite: "The term thickness is understood by those of skill in the art as a [thickness] height of a layer in a direction transverse the layers within the semiconductor substrate," in order to clarify the term thickness. Throughout the specification the term thickness is widely used. In reading of the specification, one of skill in the art understands that thickness has to do with a height of a material and not with a width. For example if metal traces are disposed on a semiconductor substrate, the traces have properties of length, width and height, or thickness. In the art, the term thickness is clearly understood and clarified in amended paragraph [0062].

As per telephone conversations held with the Examiner on July 31st, 2003, Applicant is providing explanatory drawings (found in Attachment A) with this response in support of the facts outlined in the submitted Affidavit under 37 C.F.R. 1.132, dated March 27, 2003 and signed by Stephen J. Kovacic.

The figures submitted herewith in Attachment A illustrate two possible manufacturing options for a BJT transistor when the manufacturing steps outlined in the Yamazaki reference (U.S. Patent No. 5,955,755) are followed. Option #1 illustrates over etching of the p-type SiGe base layer, and Option #2 illustrates incomplete etching of the p-type poly Si layer. Processing steps for each of the figures A through I for Option #1 and Option #2 are also submitted in Attachment A.

The claims have been amended to clarify that which the Applicant regards as the invention. The invention as claimed is distinguished from the prior art in that the

semiconductor device which is formed has "a first layer of silicon of the second conductivity type at least substantially supported by and covering a substantial portion of the silicon and SiGe layer...where the [SiGe] first layer of silicon within the window region has a surface unaffected by a process of etching." Whereas in the semiconductor device as taught in the Yamazaki reference, the silicon layer within the window region has a surface affected by a process of etching because of the type of etchant available and because of the timed etch. As a result, semiconductor devices manufactured using the steps outlined in Yamazaki have highly variable gain characteristics across the wafer. These gain characteristics dependent upon an amount of etching into the Si base region. Thus, these devices are not manufacturable in a repeatable manner.

Claim Rejection Under 35 U.S.C. 112

Claims 30 to 32 have been rejected under 35 U.S.C. 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 30 has been amended to recite the limitation "uniform thickness profile" as opposed to controllable thickness profile. Through the process of other than etching of the first silicon layer the semiconductor device allows for substantially reproducible results to be obtained for each manufactured semiconductor device as claimed. Because the first layer of silicon within the window region has a surface unaffected by a process of etching, a uniform thickness profile is achieved, which results in the substantially reproducible results.

Claim Rejection Under 35 U.S.C. 102

Claims 10-16 and 22-29 have been rejected under 35 U.S.C. 102(a) as being anticipated by Yamazaki U.S. Patent No. 5,955,745 ('745).

Applicant would like to direct the Examiner's attention to the material submitted in Attachment A, as well as to the previously submitted Affidavit under 37 C.F.R. 1.132, dated March 27, 2003 and signed by Stephen J. Kovacic. The Applicant respectfully

submits that the Yamazaki figures 12a through 12e incorrectly reflect the semiconductor device since they fail to illustrate the etching of the silicon layer 28. The Option #1 and Option #2 figures submitted in Attachment A provide a clearer indication of etching occurring in the window region.

Independent claims 10, 13 and 30 include the limitation "the first layer of silicon having its surface unaffected by a process of etching within the window region." This limitation significantly distinguishes the invention from that of Yamazaki. With reference to the material submitted in Attachment A and the Affidavit, the Yamazaki patent cannot anticipate claims 10, 13 and 30, as well as dependent claims that are dependent thereon. Thus, claims 10 to 16, and 22 to 32 are now in allowable form.

No new matter has been added in the amended claims.

Applicant looks forward to favourable reconsideration of the present application.

Please charge any additional fees required or credit any overpayment to Deposit Account No: 50-1142.

Respectfully,

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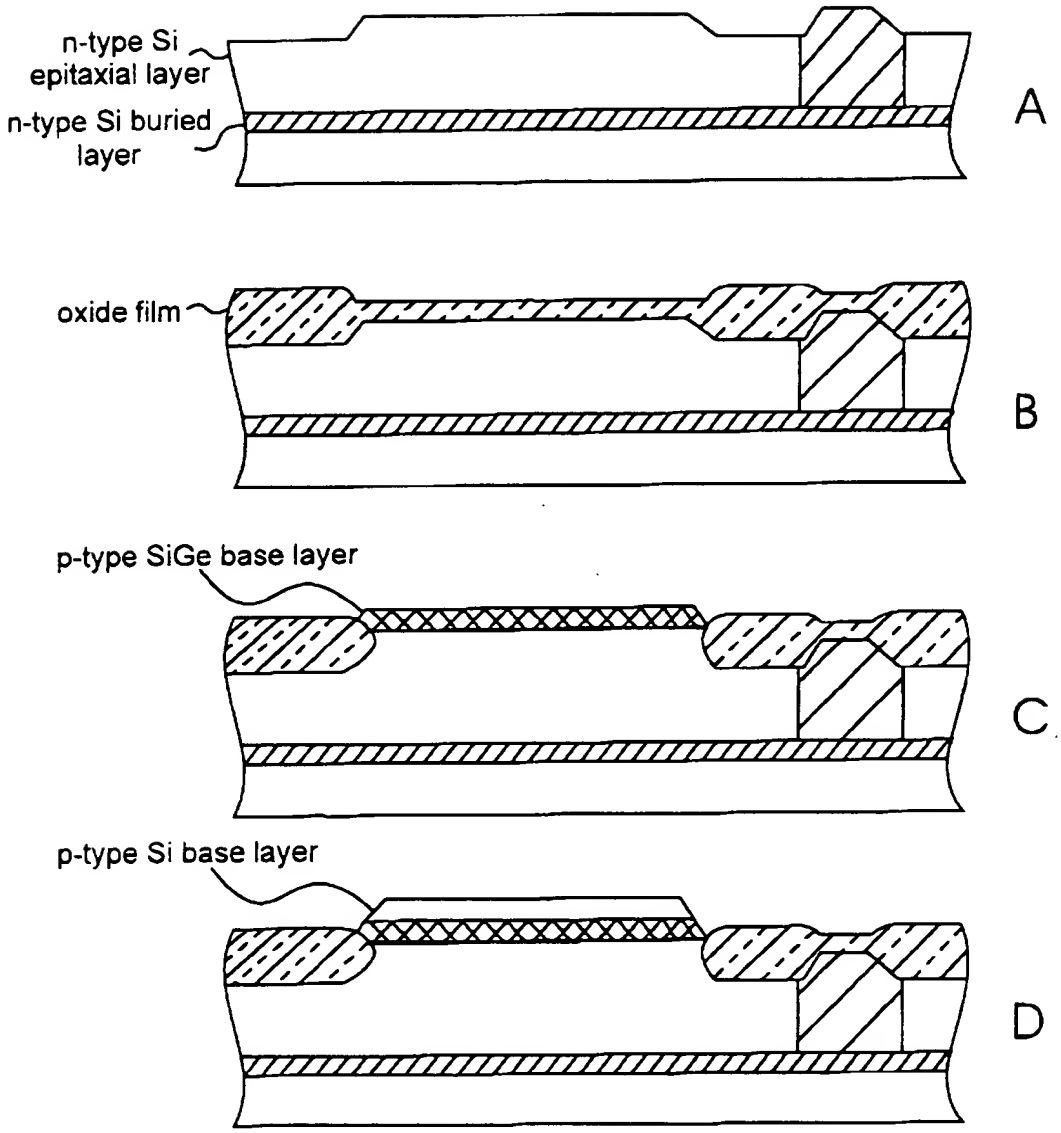
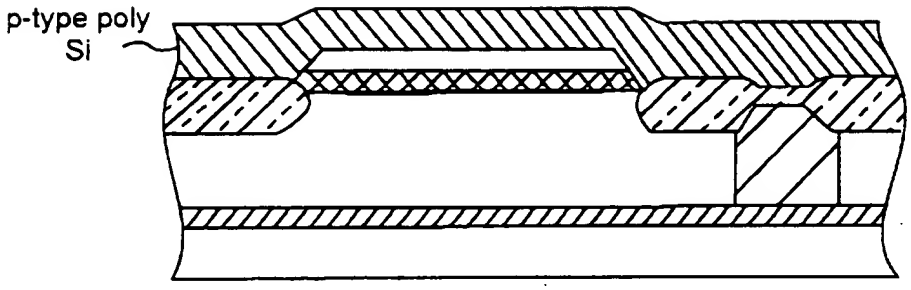
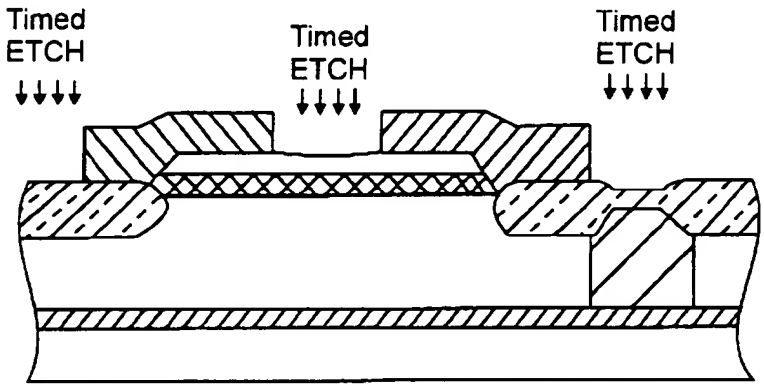
Attachment A

Option #1

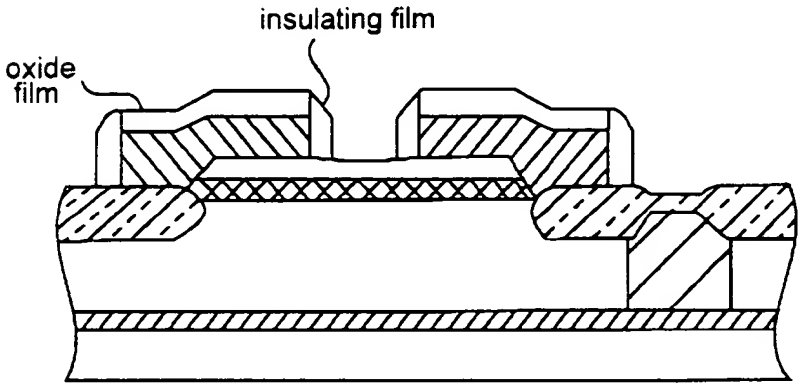

n-type Si epitaxial layer
n-type Si buried layer
A
oxide film
B
p-type SiGe base layer
C
p-type Si base layer
D


p-type poly
Si

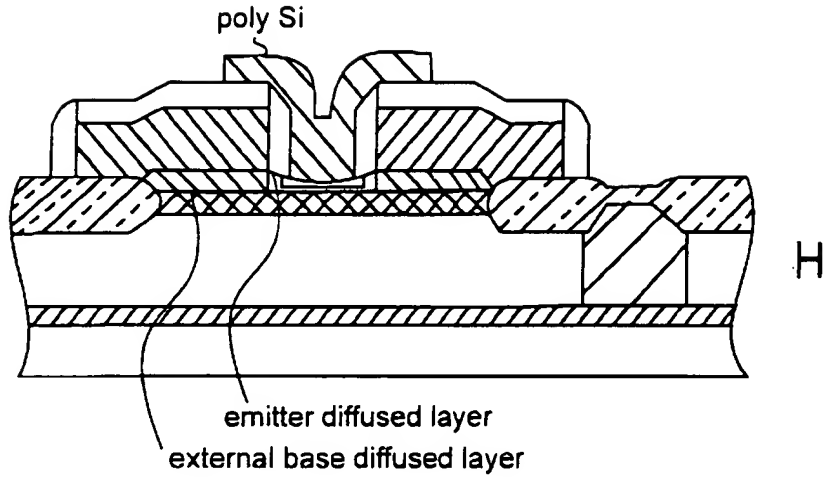
E

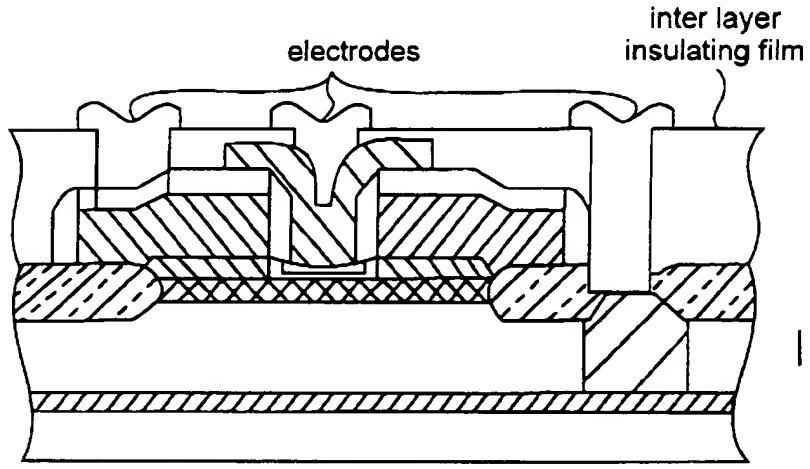

Timed
ETCH
Timed
ETCH
Timed
ETCH

F

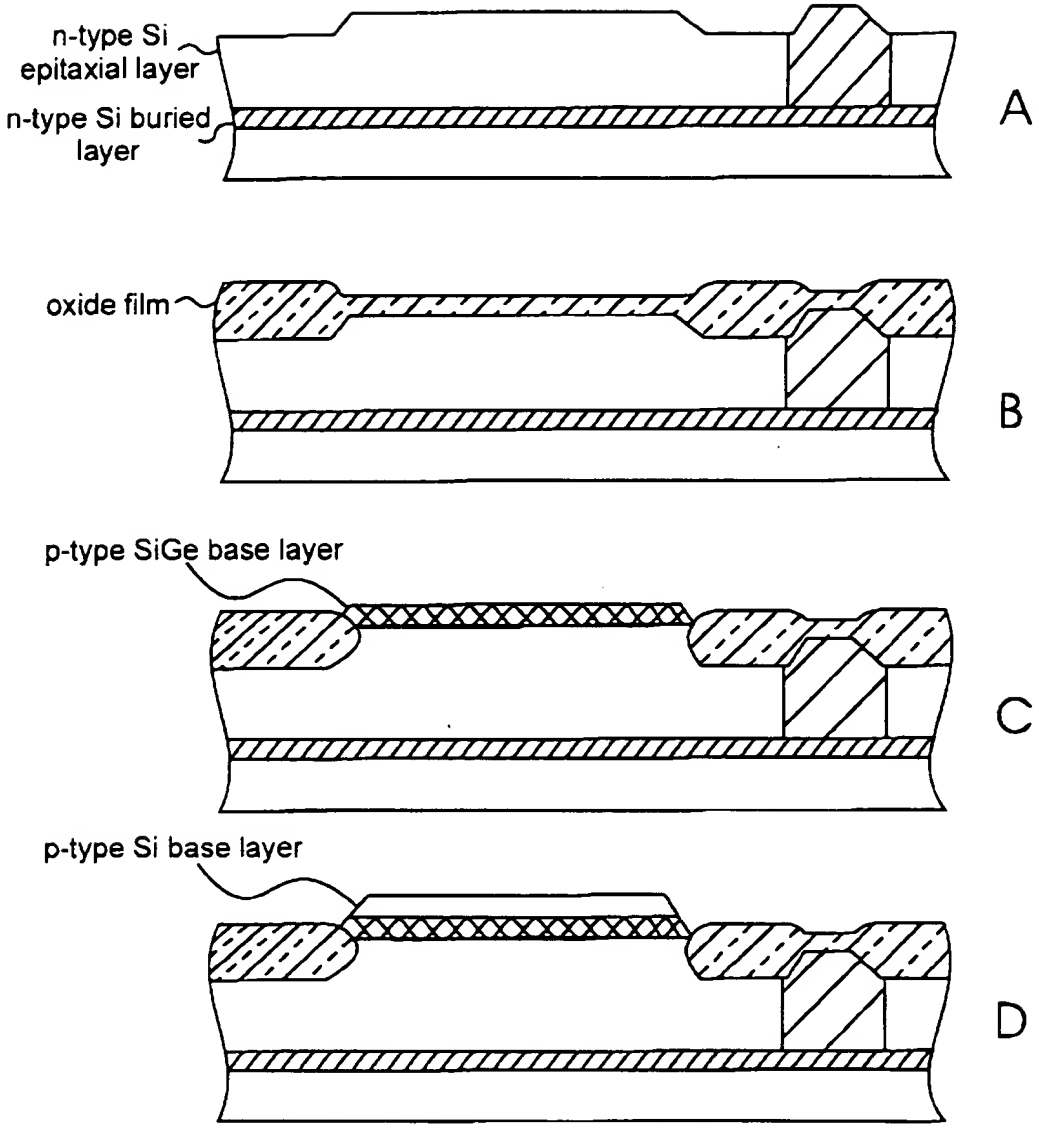

insulating film
oxide
film

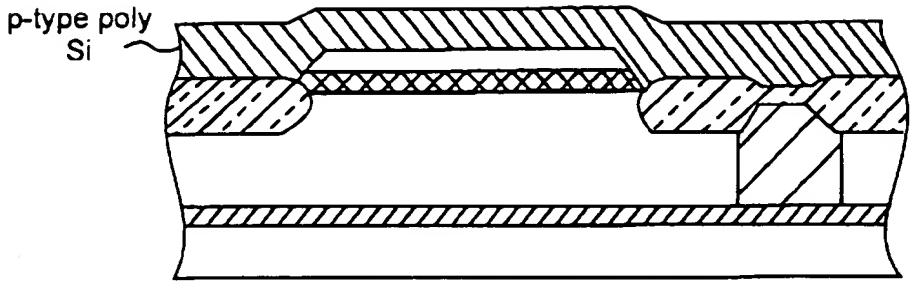
G


poly Si
emitter diffused layer
external base diffused layer
H

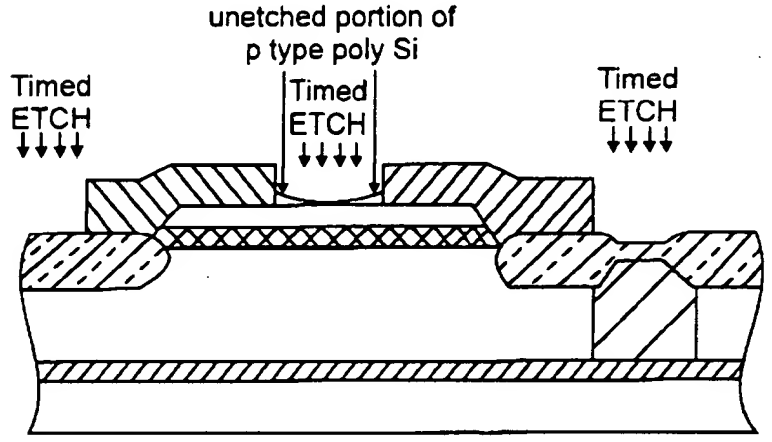

electrodes
inter layer
insulating film
I

Option #2

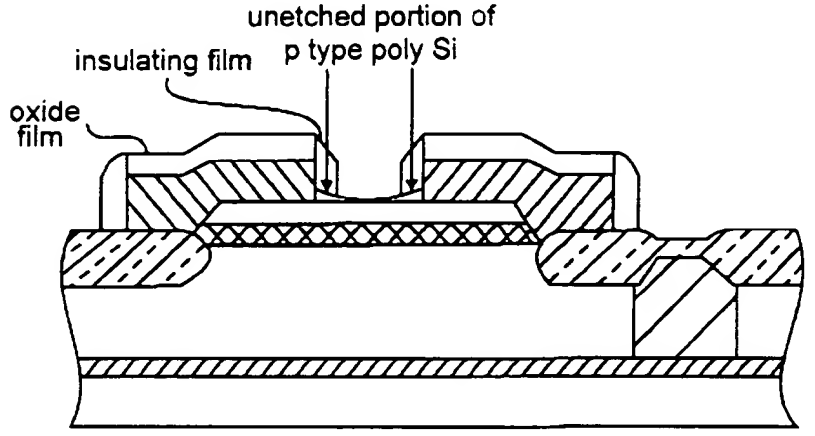

n-type Si epitaxial layer
n-type Si buried layer
A
oxide film
B
p-type SiGe base layer
C
p-type Si base layer
D


p-type poly
Si

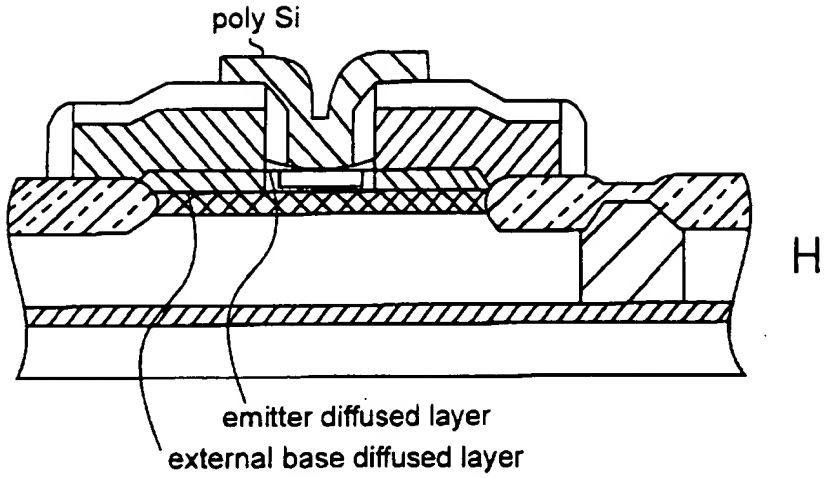
E


unetched portion of
p type poly Si
Timed
ETCH
Timed
ETCH
Timed
ETCH

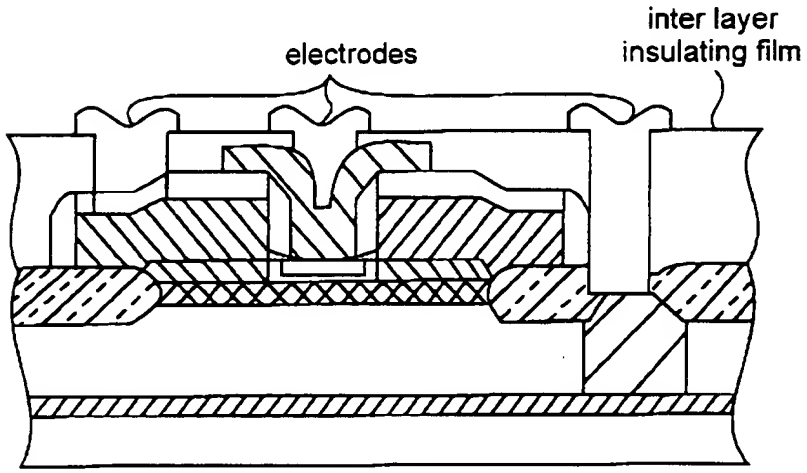
F


unetched portion of
p type poly Si
insulating film
oxide
film

G


poly Si
emitter diffused layer
external base diffused layer

H


electrodes
inter layer
insulating film

Step A:

N-type buried layer and N-type Si collector layer, a N-type epitaxial layer, are successively formed over an entire area on P-type silicon substrate.

Step B:

Isolation oxide film selectively formed using a known method on the surface of Si collector layer, the N-type epitaxial layer.

Step C:

The oxide film on the base region is removed using known photo-etching methods (step not shown). Using a selective epitaxial growth method, a SiGe spacer layer is grown on a base region in which a surface of the Si collector layer, the N-type epitaxial layer, is exposed.

Step D:

Using a selective epitaxial growth method a Si base layer, a silicon intrinsic base layer, is successively grown on the base region of the SiGe spacer layer.

Step E:

P-type polycrystalline silicon layer of 100 to 300 nm containing boron is formed over the entire area.

Step F:

Patterning of the P-type polycrystalline silicon layer takes place, where a step of timed etching selectively removes unwanted portions of the P-type polycrystalline silicon.

Unfortunately, because of the type of etchant that is available, a timed etch is necessary in order to terminate the etching process prior to having the etchant attack the underlying p-type Si base layer. As a result, this underlying layer is etched (Option #1) or not etched at all (Option #2). If this layer is not etched at all, then some of the p-type poly Si layer remains.

Step G:

An inter-layer insulating film, for example, an oxide film, is formed selectively over the p-type poly Si.

Step H:

After the insulating and oxide film are disposed, a polycrystalline silicon layer is deposited and then patterned using a photo-etching method to form an emitter electrode.

Step I:

After an emitter diffused layer and external base diffused layer are formed, inter-layer insulating film and electrodes are formed by a known method, thereby completing a bipolar transistor having gain characteristics that are highly variable across the wafer and are dependent upon the amount of etching into the Si base region.